2. (Original) The method of claim 1, wherein the low power state is a deep sleep state.

3. (Original) The method of claim 1, wherein the low power state is a C3 state.

4. (Currently Amended) The method of claim 1, wherein the memory area is coupled to a memory subsystem which does not generate snoop cycles to the processor during [any bus master accesses] the memory read operation performed by the bus master device.

5. (Currently Amended) The method of claim 4, wherein the bus master device is allowed to [generate] perform the [bus master] memory read operation [and write operations] when [the] an arbiter disable (ARB_DIS) bit is set.

6. (Currently Amended) A computer readable medium having [stored thereon sequences of] one or more associated instructions which [are executable by a system, and which], when executed [by the system, cause the system to perform a method, comprising], results in a machine performing:

setting a memory area used by a bus master device as [non-cacheable] write-through cacheable, the memory area and the bus master device are in a computer system;

enabling the bus master device to perform a [not setting a bus master status bit (BM_STS) for any bus master] memory read operation [by the bus master device with] from the memory area[; and] while keeping [placing the] a

processor in the computer system [into] in a low power state.

7. (Original) The computer readable medium of claim 6, wherein the low power state is a deep sleep state.

8. (Original) The computer readable medium of claim 6, wherein the low power state is a C3 state.

9. (Currently Amended) The computer readable medium of claim 6, wherein the memory area is coupled to a memory subsystem which does not generate snoop cycles to the processor during any [bus master] memory read operations [accesses] performed by the bus master device.

10. (Currently Amended) The computer readable medium of claim 9, wherein the bus master device is allowed to [generate bus master] perform the memory read [and write] operations when [the] an arbiter disable (ARB_DIS) bit is set.

11. (Currently Amended) A system, comprising:

a memory area set as [non-cacheable] write-through cacheable;

a bus master device coupled to the memory area; and

a processor coupled to the memory area and the bus master device, wherein the processor is placed into a low power state while the bus master device performs memory read operations with the [non-cacheable] memory area [and while a bus master status (BM_STS) bit is not set for these bus

operations].

12. (Original) The system of claim 11, wherein the low power state is a deep sleep state.

13. (Original) The system of claim 11, wherein the low power state is a C3 state.

14. (Currently Amended) The system of claim 11, further comprising a memory subsystem coupled to the memory, wherein the memory subsystem does not generate snoop cycles to the processor during any memory read operations performed by the bus master device

15. (Currently Amended) The system of claim 14, wherein the bus master device is allowed to perform the memory [generate bus master] read [and write] operations when an arbiter disable (ARB_DIS) bit is set, and when a bus master status (BM_STS) bit is not set.